MINRES TECHNOLOGIES

Building Trust: A Development Framework for High-Reliability RISC-V Subsystems

The global adoption of RISC-V based systems is accelerating rapidly, driven by open standards, adaptability to multiple applications, and vendor independence.

AI / EDGE

AUTOMOTIVE

CONSUMER / IOT

DATA CENTER

> **Choosing RISC-V as base technology represents a real paradigm shift in the product development lifecycle: systems are no longer constrained by traditional fixed processor offerings.**

RISC-V processors are tailored to each system's needs, enabling efficient hardware-software co-design. This shift enhances performance, reliability, and long-term maintainability.

MINRES addresses this fundamental transformation, leveraging a Virtual Prototyping driven methodology, centered on its **TGC (The Good Cores)** RISC-V core family, and the **MINRES Moonlight RISC-V Subsystem**. This approach to the product development provides highly automated incremental steps, allowing teams to make informed decisions on the trade-offs posed by the different development stages. The early hardware-software integration not only shifts development left but also ensures that the final product is optimally aligned with functional, safety, and security requirements.

From an industrial growth and product strategy perspective, organizations adopting a family of RISC-V processors benefit from reduced long-term support costs and improved scalability across diverse product lines.

A Strategic, Scalable Technology Foundation

RISC-V adoption is expanding rapidly world-wide, driven by applications in IoT, automotive and consumer electronics, and data center infrastructure. Forecasts predict a market in the tens of billions in the coming years, confirming that RISC-V is no longer a niche, but a global, strategic scalable technology foundation.

The global CPU market may still be dominated by ARM and x86 but the openness, extensibility and customization capabilities of RISC-V effectively reduces development costs, fosters innovation and supports a growing need to serve geopolitical sovereignty objectives.

In terms of how it's being utilized, RISC-V is moving well beyond embedded microcontrollers into high-growth, high-value segments. The key vertical market opportunities for RISC-V is expanding, including:

- **AI, High-Performance and Edge Computing**
- **Automotive:** ADAS (autonomous compute domains) and vehicle electrification
- **Consumer and IoT**
- **Data Centers and HPC** - the fastest growing sectors

Consumer and Edge IoT applications are the traditional RISC-V strongholds, due to the applications' low power requirements and the customization capabilities of RISC-V. The expansion of the technology and its applications and market opportunities is supported by a robust RISC-V ecosystem of tooling, silicon-proven IP, software support and active standardization efforts.

As with any emerging technology, RISC-V still presents some challenges, but it is no longer a risky niche endeavor. In practice, successful adoption depends on addressing a number of real or perceived obstacles through deliberate technical and organizational choices.

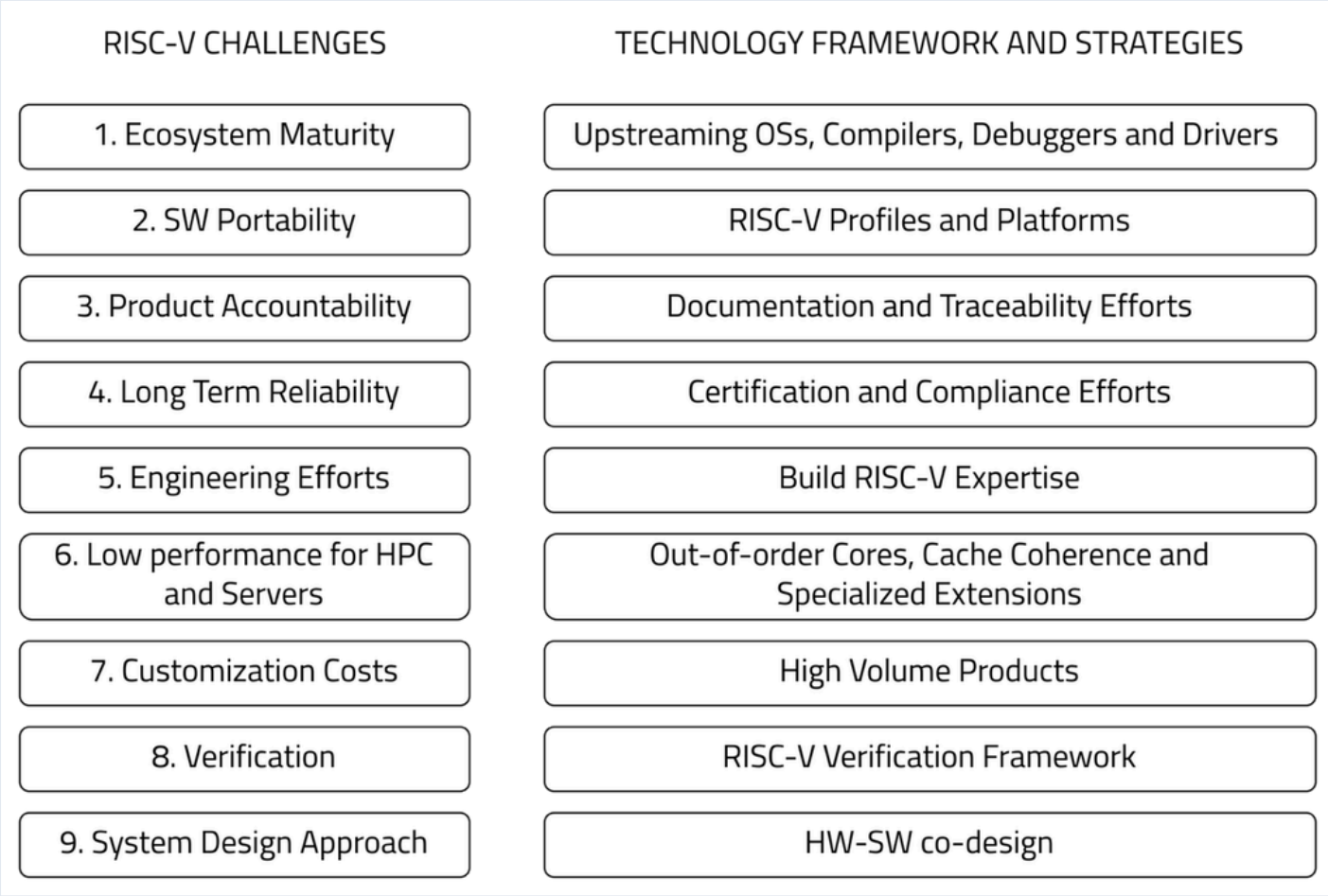


Figure: RISC-V Challenges and Technology Framework Strategies

3.1 Strengthening the Software Ecosystem

The progress of the RISC-V ecosystem is already visible in mature support for Linux, GCC/LLVM, and RTOSs, especially for embedded and edge applications. To scale industrial adoption further, the remaining software gaps in specialized domains such as AI and automotive safety need to be closed, while also improving support for common extensions, stable ABIs, and system interfaces. Short term, this can be alleviated by using turn-key SDKs. In the long term, collective action to upstream improvements to the respective projects is key to further advance the ecosystem.

3.2 Standardizing Portability

Software portability across RISC-V systems is best achieved by adopting defined profiles and platforms rather than relying on the ISA alone. Because optional extensions and implementation choices vary widely, clearly publishing the supported RISC-V profile, platform, and configuration is essential for predictability and compatibility. Proprietary extensions can increase fragmentation, upstreaming should be considered where possible.

3.3 Managing Integration & Accountability

Adopting RISC-V often means coordinating multiple IP and tool vendors, sometimes with less standardized support models. This integration complexity can be reduced through clear allocation of responsibilities, as well as disciplined documentation and traceability of requirements, processes, and results. These practices are especially important in new developments and wherever safety, security, or certification objectives must be met.

3.4 Market Perception & Readiness

Market acceptance of RISC-V can be more challenging in conservative industries with long development cycles and strong expectations regarding long-term support. In parallel, certification and compliance remain more demanding because pre-certified cores are still limited and tool qualification is not yet complete. Building confidence therefore requires a realistic perspective on the readiness of RISC-V: while RISC-V is still an emerging alternative compared to ARM or x86, its growing success in automotive, edge, IoT, HPC, and datacenter infrastructure demonstrates clear momentum and increasing readiness for demanding applications.

3.5 Building In-House Expertise

Successful RISC-V adoption benefits from building in-house expertise across microarchitecture, compilers, and low-level firmware such as HALs and BSPs. Although establishing these skills may increase short-term investment and initially slow team scaling, it is a natural consequence of adoption. In the long term it can be beneficial, not only for developing new RISC-V-based solutions, but also for integrating existing ones effectively into products.

3.6 Optimizing Predictable Performance

Careful evaluation ensures predictable performance and ROI modeling. Performance can be improved through out-of-order execution, cache coherence, and dedicated extensions, based on representative real workloads rather than synthetic benchmarks.

3.7 Design Customization

Customization is one of the main strengths of RISC-V, but it should be applied with clear economic and technical discipline. A highly customized solution may reduce software portability and increase maintenance effort, potentially creating forked ecosystems and higher support demands. These trade-offs are best justified where product volume or differentiation makes the additional hardware and software investment worthwhile. Furthermore, the effort required for customization can be reduced through the use or development of automated flows that apply the necessary adaptations consistently across all relevant areas.

3.8 A Realistic View of Openness

A successful RISC-V strategy requires a clear understanding of what “open” actually means in practice. An open ISA does not automatically eliminate license fees across the value chain, nor does it remove costs for software porting, toolchain adaptation, verification, or ecosystem development. At the same time, openness enables implementers to audit the development process more directly, and reliability and security can be strengthened through shared verification frameworks, formal methods, and standard security extensions.

3.9 Co-Design as a Principle

RISC-V adoption is most effective when hardware and software are developed together from the beginning. Focusing only on hardware innovation first can delay achieving expected capabilities. A co-design approach encourages system-level thinking and is supported by early access to toolchains and reference BSPs.

Considering all these factors, the challenges of adopting RISC-V can be addressed by using standardized platforms where portability matters and software dependence is high, while applying customization where differentiation creates value.

Software-Driven Hardware Design

Our work approach at MINRES is driven by the motivation to enable teams to find the optimal System-on-Chip solution for their needs, while at the same time meeting the growing needs on reliability and trustworthiness, and competitive schedules. This calls for a software-driven approach to develop RISC-V solutions, that relies on trusted design methodologies, proven expertise, flexible and reliable IP and state-of-the-art tools.

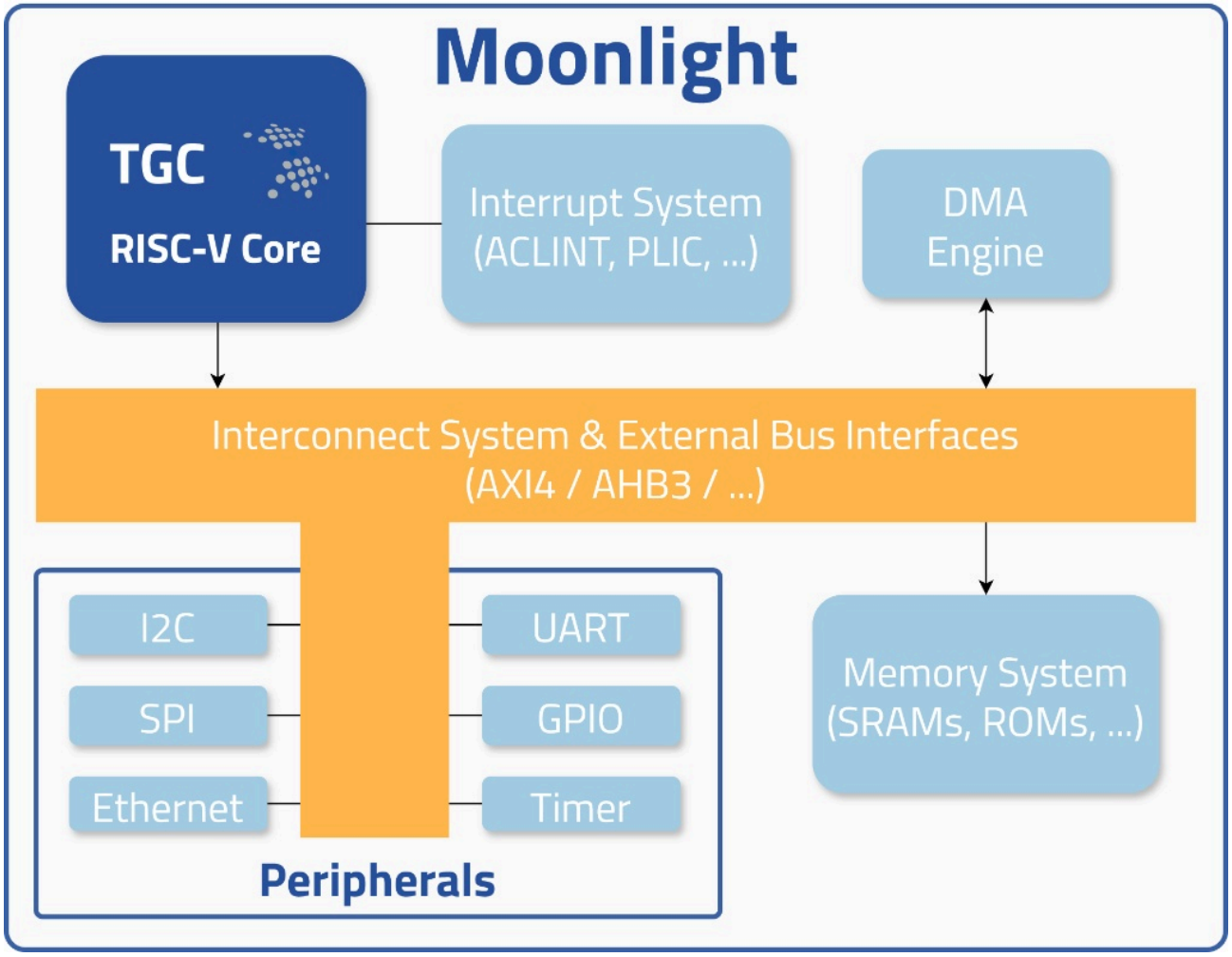
The traditionally long hardware development lifecycle is constantly being challenged by the pressure of continuous innovation and tight time-to-market schedules, which makes not only the development time an issue, but also requires taking the right decisions as early as possible.

To overcome these challenges and enable software-driven hardware design, we at MINRES offer a solution combining state-of-the-art techniques with innovative tools: **Our customizable RISC-V subsystem called Moonlight.**

4.1 Moonlight RISC-V Subsystem

At the center of Moonlight lies MINRES TGC (The Good Core), a pre-verified and pre-packaged RISC-V processor family developed and maintained by MINRES. TGC is accompanied by a wide range of proven and configurable peripherals, adapted to the specific requirements of the application. Finally, Moonlight features the required interconnect and infrastructure options, as well as the tools to build the complete subsystem with the desired options.

This hardware platform is accompanied by our VP (Virtual Prototype), a representation of Moonlight. The VP enables software-driven hardware design, shortening the overall development lifecycle and ensuring the hardware subsystem meets the software requirements.



MINRES Moonlight RISC-V Subsystem Core Components

4.2 TGC (The Good Core)

The MINRES TGC is a pre-verified and pre-packaged RISC-V processor family developed and maintained by MINRES. The cores of our TGC family cover a wide range, from low-power embedded systems up to multi-issue out-of-order cores for the most demanding high-performance applications. All TGC cores also offer additional customization options; this includes security features (ECC, parity, lockstep), tracing and debugging capabilities, cache support, user mode and more.

Furthermore, they can also be extended with custom instructions: Our automatic flow for ISAXes (ISA eXtensions) facilitates exploring and integrating custom instructions, allowing the cores to be optimized for the application.

4.3 Peripherals

Moonlight is available with a range of standard peripherals, covering the most common needs. This can include GPIO, UART, Timer, I2S, (Quad-)SPI, Ethernet (Quad-)SPI, I2C, I3C, USB2, USB3. These peripherals are proven and ready to use; they can also be configured to the specific needs. Other (custom) peripherals are of course also possible, either by integrating an existing IP or created from scratch.

4.4 Infrastructure & Configurability

Finally, Moonlight comes with a range of infrastructure components. These include interconnects for connecting the various peripherals, TGC and other components; various memory options for RAM and ROM; and a configurable DMA engine. To bring all those parts together, the MINRES tooling allows to define and configure the various aspects: Which TGC and which peripherals are used, how the connections between should be set up - including which bus protocols to use - as well as configuring the individual peripherals and other components. Supported protocols include:

- **AMBA protocols:** APB, AHB3, AXI4, AXI4Lite
- **OCP, OBI**

4.5 Virtual Prototyping

The RISC-V subsystem virtual prototype is a fully functional software representation of the hardware functionality. Initially, it can be loosely timed for early software development and later refined into an approximately timed model to allow architectural exploration. The VP is an important factor for the iterative development flow.

4.6 MINRES RAVEN

RAVEN is an advanced verification and simulation framework from MINRES; it can be used with virtual prototypes, including the VP of Moonlight. The main benefit of RAVEN is that it speeds up SystemC simulations by partitioning the VP, increasing the productivity for testing and verification.

RAVEN also supports Hybrid Simulation: While parts of the system are still simulated using SystemC, other parts are instead emulated on an FPGA. This can further improve simulation performance, when performance intensive parts of the simulation are moved to the FPGA. Furthermore, it allows the developer to integrate hardware components into the SystemC simulation. Either when no SystemC model is available; or to increase accuracy by using the original HDL. So, to summarize the benefits of using MINRES RAVEN: it automates the time-consuming and error-prone steps to build a hybrid simulation setup.

4.7 Iterative Development Flow

Finding the most suitable RISC-V subsystem for a product is done interactively by means of highly automated and reproducible processes and tools that conform to MINRES design and verification flow. The safety-aware design flow takes the product requirements as input to start the software customization on the initial RISC-V subsystem design.

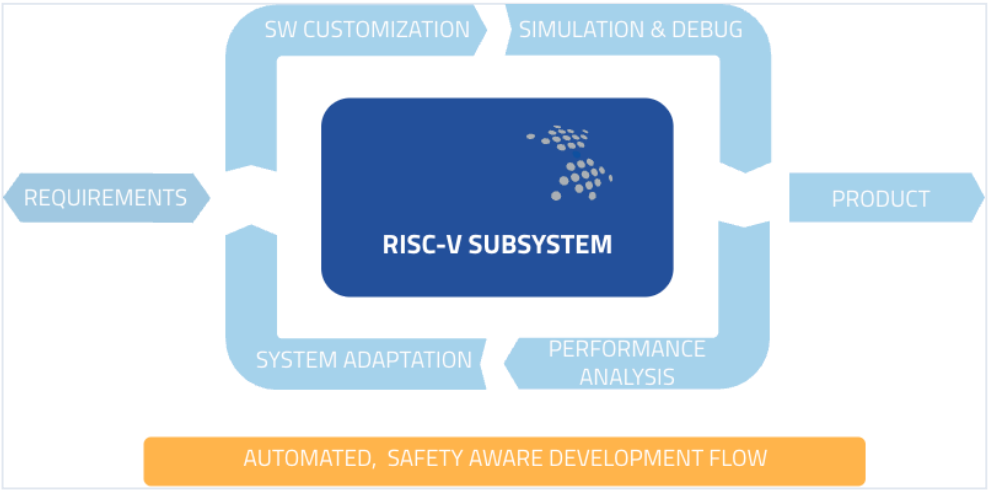


Figure: Automated, Safety Aware Development Flow

Typically this process starts with using the Moonlight VP, which enables rapid prototyping and design exploration. These insights can then be used as an input for generating configurations of the Moonlight HW platform, where the insights can be validated and refined.

This approach allows timely and accurate adjustments of the design to suit KPI trade-offs and evolving requirements. The early integration of hardware and software enables a considerable shift-left with increased levels of automation and efficiency in the development cycle, while at the same time ensures a final product that is best suited to the intended functionality. Furthermore, the resulting product meets the highly demanding safety and security standards required in fields like automotive, space or aviation, where the solutions require for example post-quantum computing capabilities or machine learning software acceleration.

Example Use Cases

The configurability of Moonlight enables it to be used for a wide range of different applications. Here we provide exemplary public projects:

Scale4Edge (Scalable Edge AI)

The goal of the Scale4Edge research project was to develop a scalable edge AI platform using RISC-V; this is achieved by both combining the RISC-V core with AI accelerators, but also using custom ISA extensions. The MINRES TGC family is central part of this project, providing configurable RISC-V cores to be used for the AI platform. Moonlight as a whole was used as a reference platform surrounding the RISC-V core and AI accelerators. The configurability and flexibility were important here, for example, to simplify the addition of new peripherals. The Moonlight VP was used as a tool to facilitate early design space exploration and to validate the hardware platform implementation against the VP.

TRISTAN (European RISC-V Ecosystem)

The central goal of the TRISTAN project was to “expand, mature and industrialize” the European RISC-V ecosystem. A library of reusable building blocks for SoC design was set up to cover the whole ecosystem of SoC development, including hardware IP, EDA tools as well as software components. The MINRES Moonlight subsystem is part of this library and provides a wide range of high-quality IP from various application domains. Moonlight’s extendibility facilitates the straightforward integration of these - or other - building blocks.

DAEDALUS (Avionics SATCOM)

The European DAEDALUS project aims to develop next-generation SATCOM systems for future fighter jets. Moonlight is used as the central management and control system; responsible for both controlling the rest of the system, as well as encrypting and decrypting traffic. As DAEDALUS is a research project, Moonlight’s configurability makes it easier to assess the impact of different options and implementations. The custom instruction capabilities of the TGC family enable the efficient execution of post-quantum cryptography (PQC) algorithms, and the Moonlight VP also enables the developer to evaluate design space on a platform level.

Mannheim-FlexKI (Automotive/Industrial AI)

One of the main objectives of Mannheim-FlexKI was to develop a flexible hardware platform for AI acceleration, with a focus on automotive and industrial use cases. MINRES IP is deployed in two places: firstly, RISC-V cores from the TGC family are used in the compute-clusters for handling computation tasks, with custom instructions allowing optimization for specific use cases such as AI inference. Secondly, Moonlight is used as the ‘control-cluster’ which acts as the entry point of the chip, booting and setting up the rest of the system while also providing external connections and peripherals. Moonlight’s configurability enabled the easy integration of a custom peripheral for an external camera interface.

De-risk and Accelerate Your RISC-V Strategy

The RISC-V challenges described in this paper are effectively addressed by the features and methodologies presented by MINRES and this allows our customers and partners to de-risk and to accelerate their move towards a more efficient and scalable RISC-V based product strategy and implementation.

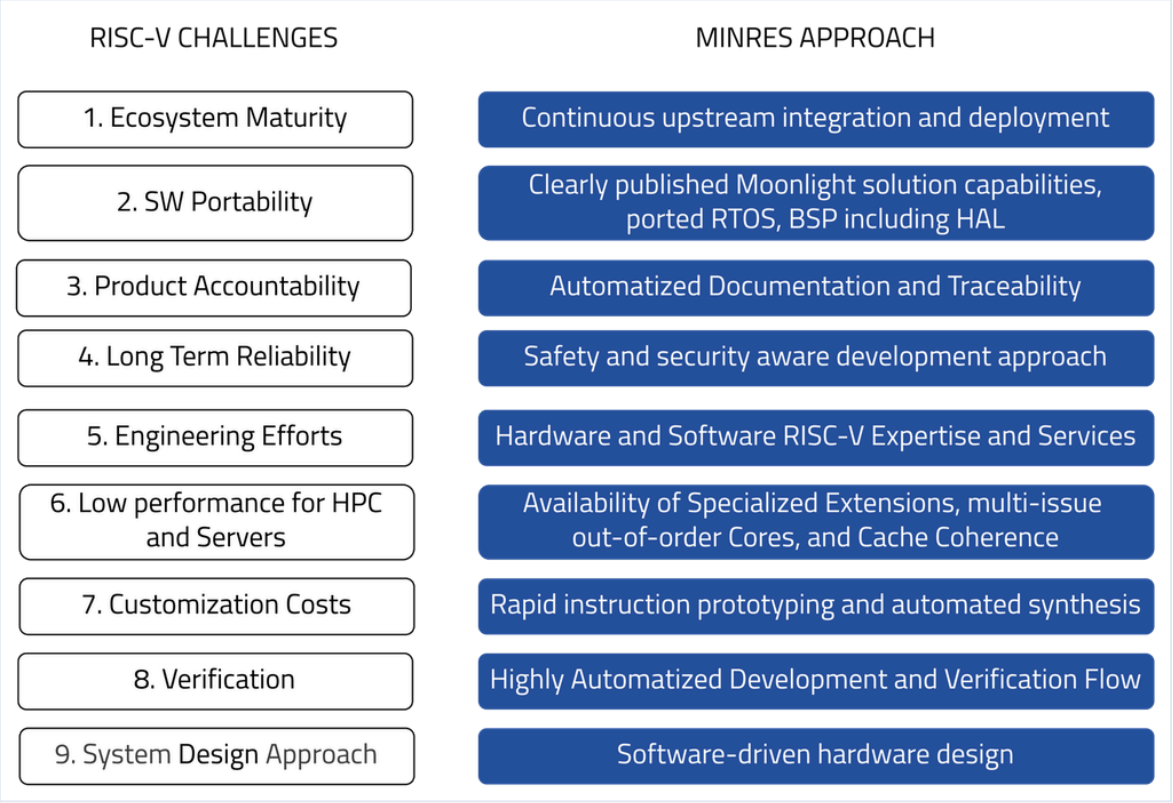


Figure: Addressing RISC-V Challenges with the MINRES Approach

In summary, the MINRES approach with our TGC RISC-V cores and Moonlight subsystem addresses the challenges of adopting RISC-V by providing:

- A software-driven hardware design methodology
- Pre-verified, customizable RISC-V cores (MINRES TGC)
- A flexible, reliable subsystem architecture (MINRES Moonlight)
- A robust verification framework (MINRES Raven)
- Automated, reproducible development flows

Ready to optimize your System-on-Chip solution?

If some of the challenges and solutions presented here sound familiar, contact MINRES to find out how our experienced team can support your development requirements.